AMENDMENTS TO THE CLAIMS

Please amend the Title of the Invention as follows:

~~PCRAM CELL OPERATION METHOD~~ MEMORY DEVICE AND METHODS ~~TO CONTROL ON/OFF~~ OF CONTROLLING RESISTANCE VARIATION AND RESISTANCE PROFILE DRIFT

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior listing of claims for the present application.

1. (Currently amended) A method for controlling resistance variation in a variable resistance memory device, the method comprising:

a) ~~categorizing~~ determining a variable resistance memory cell ~~as being~~ to be in either an "on" state or an "off" state based on a resistance ~~level~~ of the memory cell;

b) if the memory cell is ~~categorized as being~~ determined to be in the "on" state, determining if the resistance ~~level~~ of the memory cell is outside a predetermined resistance range for the "on" state;

c) if the memory cell is categorized as being in the "off" state, determining if the resistance ~~level~~ of the memory cell is outside a predetermined resistance range for the "off" state; and

d) ~~applying a reset pulse to the memory cell to restore an original resistance profile of the memory cell~~ shifting the resistance of said memory cell to said predetermined resistance range for either the "on" or "off" state by applying at least one reset pulse to said memory cell if the condition tested for in either b) or c) is determined to exist in the memory cell.

2. (Currently amended) The method according to claim 1, wherein said act of determining if the resistance ~~level~~ of the memory cell is outside a predetermined resistance range for the "on" state ~~includes~~ further comprises determining if the resistance ~~level~~ of the memory cell is greater than a predetermined maximum resistance ~~level~~ for the "on" state.

3. (Currently amended) The method according to claim 2, wherein the at least one reset pulse applied to the memory cell is a "hard" write pulse ~~for restoring an original resistance level for the "on" state~~ if the resistance ~~level~~ of the memory cell is greater than the predetermined maximum resistance.

4. (Currently amended) The method according to claim 3, wherein the "hard" write pulse ~~is in the form of a pulse having at least one of~~ has a voltage magnitude greater than a ~~predetermined~~ threshold voltage ~~level~~ of a programming ~~normal~~ write signal and a pulse width greater than that of ~~a predetermined pulse width of a normal~~ said programming write signal.

5. (Currently amended) The method according to claim 2, wherein the at least one reset pulse applied to the memory cell is at least one "soft" write pulse ~~for restoring an original resistance level for the "on" state~~ if the resistance ~~level~~ of the memory cell is greater than the predetermined maximum resistance.

6. (Currently amended) The method according to claim 5, wherein the "soft" write pulse ~~is in the form of a pulse having at least one of~~ has a voltage magnitude less than a ~~predetermined~~ threshold voltage ~~level~~ of a ~~normal~~ programming write signal and a pulse width less than that of a ~~predetermined~~ pulse width of ~~a normal~~ said programming write signal.

7. (Currently amended) The method according to claim 1, wherein said act of determining if the resistance ~~level~~ of the memory cell is outside a predetermined resistance range for the "on" state ~~includes~~ further comprises determining if the resistance ~~level~~ of the memory cell is less than a predetermined minimum resistance ~~level~~ for the "on" state.

8. (Currently amended) The method according to claim 7, wherein the at least one reset pulse applied to the memory cell is at least one "soft" erase pulse for restoring an original resistance level for the "on" state if the resistance level of the memory cell is less than the predetermined minimum resistance.

9. (Currently amended) The method according to claim 8, wherein the at least one "soft" write erase pulse is in the form of a pulse having at least one of has a voltage magnitude less than a predetermined threshold voltage level of a normal programming erase signal and a pulse width less than that of a predetermined pulse width of a normal said programming erase signal.

10. (Currently amended) The method according to claim 1, wherein said act of determining if the resistance level of the memory cell is outside a predetermined resistance range for the "off" state includes further comprises determining if the resistance level of the memory cell is less than a predetermined minimum resistance level for the "off" state.

11. (Currently amended) The method according to claim 10, wherein the at least one reset pulse applied to the memory cell is a "hard" erase pulse for restoring an original resistance level for the "off" state if the resistance level of the memory cell is less than the predetermined minimum resistance.

12. (Currently amended) The method according to claim 11, wherein the "hard" erase pulse is in the form of a pulse having at least one of has a voltage magnitude greater than a predetermined threshold voltage level of a normal programming erase signal and a pulse width greater than that of a predetermined pulse width of a normal said programming erase signal.

13. (Canceled).

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14. (Canceled).

15. (Currently amended) The method according to claim 1, wherein said act of determining if the resistance ~~level~~ of the memory cell is outside a predetermined resistance range for the "off" state ~~includes~~ further comprises determining if the resistance ~~level~~ of the memory cell is greater than a predetermined maximum resistance ~~level~~ for the "off" state.

16. (Currently amended) The method according to claim 15, wherein the at least one reset pulse applied to the memory cell is at least one "soft" write pulse ~~for restoring an original resistance level for the "off" state~~ if the resistance ~~level~~ of the memory cell is greater than the predetermined maximum resistance.

17. (Currently amended) The method according to claim 16, wherein the at least one "soft" write pulse ~~is in the form of a pulse having at least one of~~ has a voltage magnitude less than a ~~predetermined~~ threshold voltage ~~level~~ of a ~~normal~~ programming write signal and a pulse width less than that of a ~~predetermined~~ pulse width of ~~a normal~~ said programming write signal.

18. (Original) The method according to claim 1, wherein acts a) through d) are performed at a predetermined frequency during operation of a processor device.

19. (Original) The method according to claim 1, wherein the memory cell is a PCRAM cell.

20. (Currently amended) The method according to claim 19, wherein the PCRAM cell ~~includes~~ comprises a silver selenide layer.

21.   (Currently amended)   The method according to claim 1, further comprising:

e) prior to ~~categorizing~~ said act of determining the variable resistance memory cell to be in either an "on" or an "off" state, selecting the memory cell from among an array of variable resistance memory cells; and

f) repeating acts ~~e) and~~ a) through [[d)]] e) for ~~another~~ a second memory cell within the array of variable resistance memory·cells.

22.   (Currently amended)   The method according to claim 21, further comprising performing a plurality of write/erase cycles in the array of variable resistance memory cells during operation of a processor device, and wherein the acts of ~~e),~~ a) through ~~d) and~~ f) are performed together at a predetermined frequency during the operation of [[a]] said processor device.

23. (Currently amended) A method [[for]] of controlling [[a]] an undererase drift condition ~~towards an overly low resistance in a high resistance state~~ in a variable resistance memory cell, comprising:

a) comparing the resistance ~~level~~ of the memory cell with a reference resistance range ~~level~~ and identifying the memory cell as being [[in]] programmed to a high resistance state if the resistance ~~level~~ is above the reference resistance range ~~level~~;

b) if the memory cell is identified as being [[in]] programmed to the high resistance state, comparing the resistance ~~level~~ of the memory cell with a predetermined minimum resistance ~~level~~; and

c) if the resistance ~~level~~ of the memory cell is not greater than the predetermined minimum resistance ~~level~~, applying [[a]] at least one reset pulse to the

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memory cell to ~~restore~~ <u>shift the memory cell to</u> an original resistance ~~level~~ <u>range</u> for the high resistance state of the memory cell.

24. (Currently amended) The method according to claim 23, wherein the <u>at least one</u> reset pulse is a "hard" reset pulse ~~applied in a direction~~ <u>of sufficient magnitude and/or duration</u> to ~~raise~~ <u>increase</u> the resistance ~~level~~ <u>of the memory cell</u> in the high resistance state ~~above~~ <u>to greater than</u> the predetermined minimum resistance ~~level~~.

25. (Currently amended) The method according to claim 23, wherein the <u>at least one</u> reset pulse is at least one "soft" reset pulse ~~applied in a direction~~ <u>of sufficient magnitude and/or duration</u> to ~~raise~~ <u>increase</u> the resistance ~~level~~ <u>of the memory cell</u> in the high resistance state ~~above~~ <u>to greater than</u> the predetermined minimum resistance ~~level~~.

26. (Original) The method according to claim 23, wherein the memory cell is a PCRAM cell.

27. (Currently amended) The method according to claim 24, wherein the PCRAM cell ~~includes~~ <u>comprises</u> a silver selenide layer.

28. (Currently amended) A method [[for]] <u>of</u> controlling [[a]] <u>an underwrite</u> drift condition ~~towards an overly high resistance in a low resistance state~~ in a variable resistance memory cell, comprising:

a) comparing a resistance ~~level~~ of the memory cell with a reference ~~level~~ <u>resistance range</u> and identifying the memory cell as being [[in]] <u>programmed to</u> a low resistance state if the resistance ~~level~~ is below the reference ~~level~~ <u>resistance range</u>;

b) if the memory cell is identified as being [[in]] programmed to the low resistance state, comparing the resistance level of the memory cell with a predetermined maximum resistance level; and

c) if the resistance level of the memory cell is not less than the predetermined maximum resistance level, applying [[a]] at least one reset pulse to the memory cell to restore shift the memory cell to an original resistance level range for the low resistance state of the memory cell.

29. (Currently amended) The method according to claim 28, wherein the at least one reset pulse is a "hard" reset pulse applied in a direction of sufficient magnitude and duration to lower decrease the resistance of the memory cell level in the low resistance state below to lower than the predetermined maximum resistance level.

30. (Currently amended) The method according to claim 28, wherein the at least one reset pulse is at least one "soft" reset pulse applied in a direction of sufficient magnitude and duration to lower decrease the resistance of the memory cell level in the low resistance state below to lower than the predetermined maximum resistance level.

31. (Original) The method according to claim 28, wherein the memory cell is a PCRAM cell.

32. (Currently amended) The method according to claim 31, wherein the PCRAM cell includes comprises a silver selenide layer.

33. (Currently amended) A method [[for]] of controlling [[a]] an overerase drift condition towards an excessively high resistance in a high resistance state in a variable resistance memory cell, comprising:

a) comparing the resistance ~~level~~ of the memory cell with a reference ~~level~~ <u>resistance range</u> and identifying the memory cell as being [[in]] <u>programmed to</u> a high resistance state if the resistance ~~level~~ is above the reference ~~level~~ <u>resistance range</u>;

b) if the memory cell is identified as being [[in]] <u>programmed to</u> the high resistance state, comparing the resistance ~~level~~ of the memory cell with a predetermined maximum resistance ~~level~~; <u>and</u>

c) if the resistance ~~level~~ of the memory cell is ~~not less~~ <u>greater</u> than the predetermined maximum resistance ~~level~~, applying [[a]] <u>at least one</u> reset pulse to the memory cell to ~~restore~~ <u>shift the memory cell to</u> an original resistance ~~level~~ <u>range</u> for the high resistance state of the memory cell.

34. (Currently amended) The method according to claim 33, wherein the <u>at least one</u> reset pulse is a "hard" reset pulse ~~applied in a direction~~ <u>of sufficient magnitude and duration</u> to ~~lower~~ <u>decrease</u> the resistance ~~level~~ <u>of the memory cell</u> in the high resistance state ~~below~~ <u>to lower than</u> the predetermined maximum resistance ~~level~~.

35. (Currently amended) The method according to claim 33, wherein the <u>at least one</u> reset pulse is at least one "soft" reset pulse ~~applied in a direction~~ <u>of sufficient magnitude and duration</u> to ~~lower~~ <u>decrease</u> the resistance ~~level~~ <u>of the memory cell</u> in the high resistance state ~~below~~ <u>to lower than</u> the predetermined maximum resistance ~~level~~.

36. (Original) The method according to claim 33, wherein the memory cell is a PCRAM cell.

37. (Currently amended) The method according to claim 36, wherein the PCRAM cell ~~includes~~ <u>comprises</u> a silver selenide layer.

38. (Currently amended) A method [[for]] of controlling [[a]] an overwrite drift condition towards an excessively low resistance in a low resistance state in a variable resistance memory cell, comprising:

a) comparing a resistance level of the memory cell with a reference level resistance range and identifying the memory cell as being [[in]] programmed to a low resistance state if the resistance level is below the reference level resistance range;

b) if the memory cell is identified as being [[in]] programmed to the low resistance state, comparing the resistance level of the memory cell with a predetermined minimum resistance level; and

c) if the resistance level of the memory cell is [[not]] greater than the predetermined minimum resistance level, applying [[a]] at least one reset pulse to the memory cell to restore shift the memory cell to an original resistance level range for the low resistance state of the memory cell.

39. (Currently amended) The method according to claim 38, wherein the at least one reset pulse is a "hard" reset pulse applied in a direction of sufficient magnitude and duration to raise increase the resistance level of the memory cell in the low resistance state above to greater than the predetermined minimum resistance level.

40. (Currently amended) The method according to claim 38, wherein the at least one reset pulse is at least one "soft" reset pulse applied in a direction of sufficient magnitude and duration to raise increase the resistance level of the memory cell in the low resistance state above to greater than the predetermined minimum resistance level.

41. (Original) The method according to claim 38, wherein the memory cell is a PCRAM cell.

42. (Currently amended) The method according to claim 41, wherein the PCRAM cell ~~includes~~ comprises a silver selenide layer.

43. (Currently amended) A method for operating a PCRAM memory device ~~including an array of variable resistance memory cells~~, comprising:

determining ~~that~~ if a resistance ~~level~~ of a PCRAM memory cell [[in]] programmed to a high resistance state has deviated from an ~~initial~~ original resistance ~~level~~ range for a high resistance state thereof; and

applying at least one voltage potential to the PCRAM memory cell to ~~restore~~ shift the PCRAM memory cell to within the ~~initial~~ original resistance ~~level~~ range for the high resistance state.

44. (Original) The method according to claim 43, wherein the at least one voltage potential applied is a "hard" erase pulse.

45. (Canceled).

46. (Original) The method according to claim 43, wherein the at least one voltage potential applied is at least one "soft" write pulse.

47. (Currently amended) The method according to claim 43, wherein the at least one voltage potential is applied when the resistance ~~level~~ of the PCRAM memory cell is determined to have deviated from the ~~initial~~ original resistance ~~level~~ range ~~by an amount beyond a predetermined limit~~.

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48. (Currently amended) A method for operating a PCRAM memory device ~~including an array of variable resistance memory cells~~, comprising:

determining ~~that~~ if a resistance ~~level~~ of a PCRAM memory cell [[in]] programmed to a low resistance state has deviated from an ~~initial~~ original resistance ~~level~~ range for a low resistance state thereof; and

applying at least one voltage potential to the PCRAM memory cell to ~~restore~~ shift the PCRAM memory cell to within the ~~initial~~ original resistance ~~level~~ range for the low resistance state.

49. (Original) The method according to claim 48, wherein the at least one voltage potential applied is a "hard" write pulse.

50. (Canceled).

51. (Currently amended) The method according to claim 48, wherein the at least one voltage potential applied is at least [[on]] one "soft" erase pulse.

52. (Currently amended) The method according to claim 48, wherein the at least one voltage potential is applied when the resistance ~~level~~ of the PCRAM memory cell is determined to have deviated from the ~~initial~~ original resistance ~~level~~ ~~range by an amount beyond a predetermined limit~~.

53. (Currently amended) A method for operating a PCRAM memory device ~~including an array of variable resistance memory cells~~, comprising:

determining that a resistance profile of a PCRAM memory cell has deviated from ~~an initial~~ a programmed resistance profile of the PCRAM memory cell; and

applying at least one voltage potential to the <u>PCRAM</u> memory cell to ~~restore~~ <u>shift</u> the <u>resistance of the PCRAM memory cell to the</u> ~~initial~~ <u>programmed</u> resistance profile for the <u>PCRAM</u> memory cell.

54. (Currently amended) A method [[for]] <u>of</u> operating a PCRAM memory device ~~including an array of variable resistance memory cells~~, comprising:

~~categorizing~~ <u>determining if</u> a variable resistance memory cell ~~as being in either~~ <u>is programmed to</u> an "on" state or an "off" state based on a current resistance ~~level~~ of the memory cell; and

applying at least one ~~reset~~ <u>voltage</u> pulse <u>of sufficient magnitude and/or duration</u> to the memory cell to ~~restore~~ <u>shift</u> the <u>memory cell to an</u> ~~initial~~ <u>original</u> resistance ~~profile~~ <u>range</u> for the memory cell based on the "on" or "off" state of the cell ~~and a direction of the resistance profile to be restored relative to the current resistance level of the memory cell~~.

55. (Currently amended) The method according to claim 54, wherein the at least one ~~reset~~ <u>voltage</u> pulse applied is a "hard" write pulse.

56. (Currently amended) The method according to claim 54, wherein the at least one ~~reset~~ <u>voltage</u> pulse applied is a "hard" erase pulse.

57. (Currently amended) The method according to claim 54, wherein the at least ~~on reset~~ <u>one voltage</u> pulse applied is at least one "soft" write pulse.

58. (Currently amended) The method according to claim 54, wherein the at least ~~on reset~~ <u>one voltage</u> pulse applied is at least one "soft" erase pulse.

59. (Currently amended) A memory device comprising:

an array of variable resistance memory cells; and

a controller coupled to the memory array [[and]] which periodically performs an algorithm to detect resistance profile drift in the memory cells of the array, and which restores an original resistance profile in any of said memory cells in which resistance profile drift is detected by applying at least one pulse with sufficient magnitude and/or duration to shift the current resistance of the memory cells to the original resistance profile of said memory cells.

60. (Currently amended) The memory device according to claim 59, wherein the controller controls the application of a "hard" write pulse to a memory cell in the array if the controller detects that a resistance level of the memory cell is in a low resistance state and has deviated from an original resistance level range for the low resistance state to an underwrite condition.

61. (Currently amended) The memory device according to claim 59, wherein the controller controls application of at least one "soft" [[write]] erase pulse to a memory cell in the array if the controller detects that a resistance level of the memory cell is in a low resistance state and has deviated from an original resistance level range for the low resistance state to an underwrite undererase condition.

62. (Currently amended) The memory device according to claim 59, wherein the controller controls application of [[a]] at least one "soft" erase write pulse to a memory cell in the array if the controller detects that a resistance level of the memory cell is in a [[low]] high resistance state and has deviated from an original resistance level range for the [[low]] high resistance state to an overwrite overerase condition.

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63. (Currently amended) The memory device according to claim 59, wherein the controller controls application of a "hard" erase pulse to any memory cell in the array if the controller detects that a resistance ~~level~~ of the memory cell is in a high resistance state and has deviated from an original resistance ~~level~~ <u>range</u> for the high resistance state to an ~~undererase~~ <u>overwrite</u> condition.

Claims 64-65. (Canceled).

66. (Currently amended) A processor system, comprising:

a processor for receiving and processing data;

at least one memory array of variable resistance memory cells for exchanging data with the processor; and

a controller connected to the at least one memory array, wherein the controller

manages memory access requests from the processor to the at least one memory device,

periodically performs an algorithm to detect resistance profile drift in the memory cells of the array, and

restores an original resistance profile in any memory ~~cells~~ <u>cell</u> in which resistance profile drift is detected.

67. (Currently amended) A processor system, comprising:

a processor for receiving and processing data;

at least one memory array of variable resistance memory cells for exchanging data with the processor; and

a controller connected to the at least one memory array, wherein the controller:

performs an algorithm which detects if the resistance of any of the memory cells among the array is in a high resistance state, and whether the resistance of any cells detected to be in the high resistance cells is below a predetermined minimum level or is above a predetermined maximum level for the high resistance state,

controls application of at least one reset pulse to any cells detected to be in the high resistance state and having a resistance either below the predetermined minimum level or above the predetermined maximum level to thereby restore a predetermined resistance range for the high resistance state,

detects if the resistance of any of the memory cells among the array is in a low resistance state, and whether the resistance of any cells detected to be in the low resistance state is above a predetermined maximum level or is below a predetermined minimum level for the low resistance state, and

controls application of at least one reset pulse to any cells detected to be in the low resistance state and having a resistance either

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above the predetermined maximum level or below the predetermined minimum level to thereby restore a predetermined resistance range for the low resistance state.

68. (Original) The processor system according to claim 67, wherein the controller performs the algorithm at predetermined time intervals.

69. (New) A method of controlling resistance variation in a memory cell, said method comprising:

determining if the resistance of the memory cell is outside a first predetermined resistance range corresponding to an "on" state for said memory cell, wherein if the resistance of said memory cell is outside the first predetermined resistance range, applying at least one pulse to said memory cell to shift the resistance of said memory cell to return to a resistance within said first predetermined resistance range for said "on" state.

70. (New) The method of claim 69, wherein said act of applying at least one pulse comprises applying a "hard" write pulse to said memory cell.

71. (New) The method of claim 70, wherein said "hard" write pulse is applied with a higher voltage magnitude than a programming write voltage for said memory cell.

72. (New) The method of claim 70, wherein said "hard" write pulse is applied with a longer duration than a programming write pulse for said memory cell.

73. (New) The method of claim 69, wherein said act of applying at least one pulse comprises applying a "soft" erase pulse to said memory cell.

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74. (New) The method of claim 73, wherein said "soft" erase pulse is applied with a lower voltage magnitude than a programming erase voltage for said memory cell.

75. (New) The method of claim 73, wherein said "soft" erase pulse is applied with a shorter duration than a programming erase pulse for said memory cell.

76. (New) A method of controlling resistance variation in a memory cell, said method comprising:

determining if the resistance of the memory cell is outside a first predetermined resistance range corresponding to an "off" state for said memory cell, wherein if the resistance of said memory cell is outside the first predetermined resistance range, applying at least one pulse to said memory cell to shift the resistance of said memory cell to return to a resistance within said first predetermined resistance range for said "off" state.

77. (New) The method of claim 76, wherein said act of applying at least one pulse comprises applying a "hard" erase pulse to said memory cell.

78. (New) The method of claim 77, wherein said "hard" erase pulse is applied with a higher voltage magnitude than a programming erase voltage for said memory cell.

79. (New) The method of claim 77, wherein said "hard" erase pulse is applied with a longer duration than a programming erase pulse for said memory cell.

80. (New) The method of claim 76, wherein said step of applying at least one pulse comprises applying a "soft" write pulse to said memory cell.

81. (New) The method of claim 80, wherein said "soft" write pulse is applied with a lower voltage magnitude than a programming write voltage for said memory cell.

82. (New) The method of claim 80, wherein said "soft" write pulse is applied with a shorter duration than a programming write pulse for said memory cell.

83. (New) The method according to claim 3, wherein the "hard" write pulse has a voltage magnitude greater than a threshold voltage of a programming write signal.

84. (New) The method according to claim 3, wherein the "hard" write pulse has the same voltage magnitude as a threshold voltage of a programming write signal but a pulse width greater than that of said programming write signal.

85. (New) The method according to claim 5, wherein the "soft" write pulse has a voltage magnitude less than a threshold voltage of a programming write signal.

86. (New) The method according to claim 5, wherein the "soft" write pulse has the same voltage magnitude as a threshold voltage of a programming write signal but a pulse width less than that of said programming write signal.

87. (New) The method according to claim 8, wherein the "soft" erase pulse has a voltage magnitude less than a threshold voltage of a programming erase signal.

88. (New) The method according to claim 8, wherein the "soft" erase pulse has the same voltage magnitude as a threshold voltage of a programming erase signal but a pulse width less than that of said programming erase signal.

89. (New) The method according to claim 8, wherein the "hard" erase pulse has a voltage magnitude greater than a threshold voltage of a programming erase signal.

90. (New) The method according to claim 8, wherein the "hard" erase pulse has the same voltage magnitude as a threshold voltage of a programming erase signal but a pulse width greater than that of said programming erase signal.

91. (New) The method according to claim 44, wherein the "hard" erase pulse has a voltage magnitude greater than a threshold voltage of a programming erase signal.

92. (New) The method according to claim 91, wherein the "hard" erase pulse has a pulse width greater than a threshold voltage of said programming erase signal.

93. (New) The method according to claim 44, wherein the "hard" erase pulse has the same voltage magnitude as a threshold voltage of a programming erase signal but a pulse width greater than that of said programming erase signal.

94. (New) The method according to claim 46, wherein the "soft" write pulse has a voltage magnitude less than a threshold voltage of a programming write signal.

95. (New) The method according to claim 94, wherein the "soft" write pulse has a pulse width less than a threshold voltage of said programming write signal.

96. (New) The method according to claim 46, wherein the "soft" write pulse has the same voltage magnitude as a threshold voltage of a programming write signal but a pulse width less than that of said programming write signal.

97. (New) The method according to claim 49, wherein the "hard" write pulse has a voltage greater than a threshold voltage of a programming write signal.

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98. (New) The method according to claim 97, wherein the "hard" write pulse has a pulse width greater than a threshold voltage of said programming write signal.

99. (New) The method according to claim 49, wherein the "hard" write pulse has the same voltage as a threshold voltage of a programming write signal but a pulse width greater than that of said programming write signal.

100. (New) The method according to claim 51, wherein the "soft" erase pulse has a voltage magnitude less than a threshold voltage of a programming erase signal.

101. (New) The method according to claim 100, wherein the "soft" erase pulse has a pulse width less than a threshold voltage of said programming erase signal.

102. (New) The method according to claim 51, wherein the "soft" erase pulse has the same voltage magnitude as a threshold voltage of a programming erase signal but a pulse width less than that of said programming erase signal.